What is claimed is:

1. A synchronization method for a distributed control system including a transmission unit transmitting cyclically emitted synchronization signals, a reception unit receiving and feeding synchronization signals to a clock generator via a phase regulator of a phase-locked loop, the clock generator outputting at least one subordinate clock signal having a plurality of clock pulses occuring between at least first and second synchronization signals, comprising the steps of:

   i determining an instantaneous phase error of at least one subordinate clock signal with respect to said first and second synchronization signals;

   ii calculating a substantially uniform correction value for each clock pulse of said subordinate clock signal; and

   iii correcting said subordinate clock signal based on said correction value such that said instantaneous phase error is substantially uniformly distributed over the pulses of the subordinate clock signal between said first and second synchronization signals.

2. The method of claim 1, wherein said correction value for each subordinate clock signal is calculated by dividing the instantaneous phase-regulated value by a number of clock pulses occurring between said first and second synchronization signals.

3. The method of Claim 2, wherein division is performed by a successive addition, comprising maintaining a count as to how often the desired number of subordinate clock signals as divisor fits into the instantaneous phase-regulated value as dividend.

4. The method of claim 3, wherein possible division remainders are likewise distributed virtually uniformly over each of the clock pulses of the at least one subordinate clock signal.

5. The method of claim 4, wherein the division is carried out up to a first decimal position, and a result is rounded off to an integral correction value.

6. The method of claim 5, wherein the division is carried out by successive addition displaced by one bit by multiplying by the value two, and wherein the result is used to decide whether to round up or round down, by virtue of the fact that a last addition possibly exceeding the dividend is repeated without displacement by one bit, and in case when the dividend is exceeded, the determined value is rounded down, or is otherwise rounded up.

7. The method of claim 6, wherein, after each generated subordinate clock pulse, the division is carried out between two synchronization signals for the next

subordinate clock pulse to be generated using as dividend the phase correction value reduced by the previous correction value and as divisor the value of a reduced number of subordinate clock pulses.

8. The method of Claim 7, comprising the step of integrating the instantaneous phase errors to form an integration value, an integration fraction being smaller than one, and the integration value serving as dividend for generating correction values.

9. The method of claim 8, wherein the instantaneous phase errors are corrected to a proportional value, a proportional fraction being smaller than one and the proportional value serving as dividend for generating correction values.

10. The method of claim 9, wherein the proportional fraction is greater than the integration fraction.

11. The method of claim 10, further comprising the steps of:

iv generating and downwardly dividing primary clock signals

v using said downwardly divided primary clock signals as said at least one subordinate clock signal.

12. The method of claim 1, wherein the steps of generating subordinate clock

signals and uniformly distributing an instantaneous phase-regulated value over the subordinate clock signals are performed in real time.

13. A reception unit comprising:

a means for receiving at least two synchronization signals;

b means, coupled to said receiving means, for generating subordinate clock signals for said at least two synchronization signals;

c means, coupled to said generating means, determining a set of instantaneous phase errors between said subordinate clock signals and said at least two synchronization signals;

d means, coupled to said determining means, for determining an instantaneous phase-regulated value for correcting subordinate clock signals; and

e means, coupled to said means for determining an instantaneous phase-regulated value, for correcting said subordinate clock signals between said at least two synchronization signals to make subordinate signals essentially equidistant from one another by distributing the instantaneous phase-regulated value virtually uniformly over subordinate clock signals and determining a respective correction value for each subordinate clock signal.

14. A synchronization method for a reception unit comprising the steps of:

a receiving at least first and second synchronization signals;

b generating at least one subordinate clock signal having a plurality of clock pulses between said first and second synchronization signals;

c determining instantaneous phase errors between said subordinate clock signals and said first and second synchronization signals;

d determining an instantaneous phase-regulated value for correcting said subordinate signals;

e correcting said subordinate clock signal such that the clock pulses of the subordinate clock signal are essentially equidistant from one another by applying the instantaneous phase-regulated value substantially uniformly over the clock pulses of the subordinate clock signal .